# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

# HEF4017B
# MSI
# 5-stage Johnson counter

Product specification
File under Integrated Circuits, IC04

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Philips Semiconductors

PHILIPS

# 5-stage Johnson counter

# HEF4017B
# MSI

## DESCRIPTION

The HEF4017B is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs ($O_0$ to $O_9$), an active LOW output from the most significant flip-flop ($\overline{O}_{5\text{-}9}$), active HIGH and active LOW clock inputs ($CP_0$, $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at $CP_0$ while $\overline{CP}_1$ is LOW or a HIGH to LOW transition at $\overline{CP}_1$ while $CP_0$ is HIGH (see also function table).

When cascading counters, the $\overline{O}_{5\text{-}9}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the $CP_0$ input of the next counter.

A HIGH on MR resets the counter to zero ($O_0 = \overline{O}_{5\text{-}9}$ = HIGH; $O_1$ to $O_9$ = LOW) independent of the clock inputs ($CP_0$, $\overline{CP}_1$).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

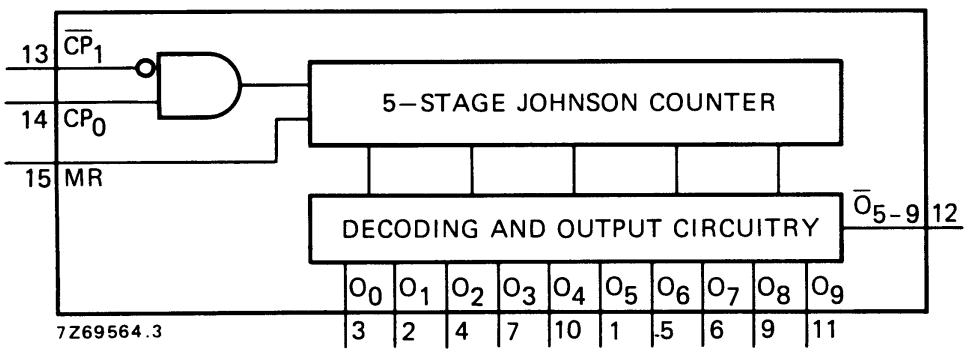



Fig.1 Functional diagram.

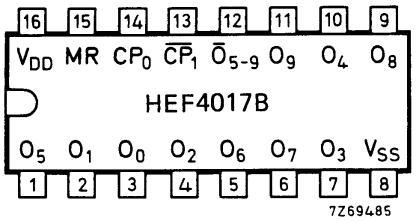



Fig.2 Pinning diagram.

## PINNING

| | |
|---|---|
| $CP_0$ | clock input (LOW to HIGH triggered) |
| $\overline{CP}_1$ | clock input (HIGH to LOW triggered) |
| MR | master reset input |
| $O_0$ to $O_9$ | decoded outputs |
| $\overline{O}_{5\text{-}9}$ | carry output (active LOW) |

## FAMILY DATA, $I_{DD}$ LIMITS category MSI

See Family Specifications

HEF4017BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4017BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4017BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

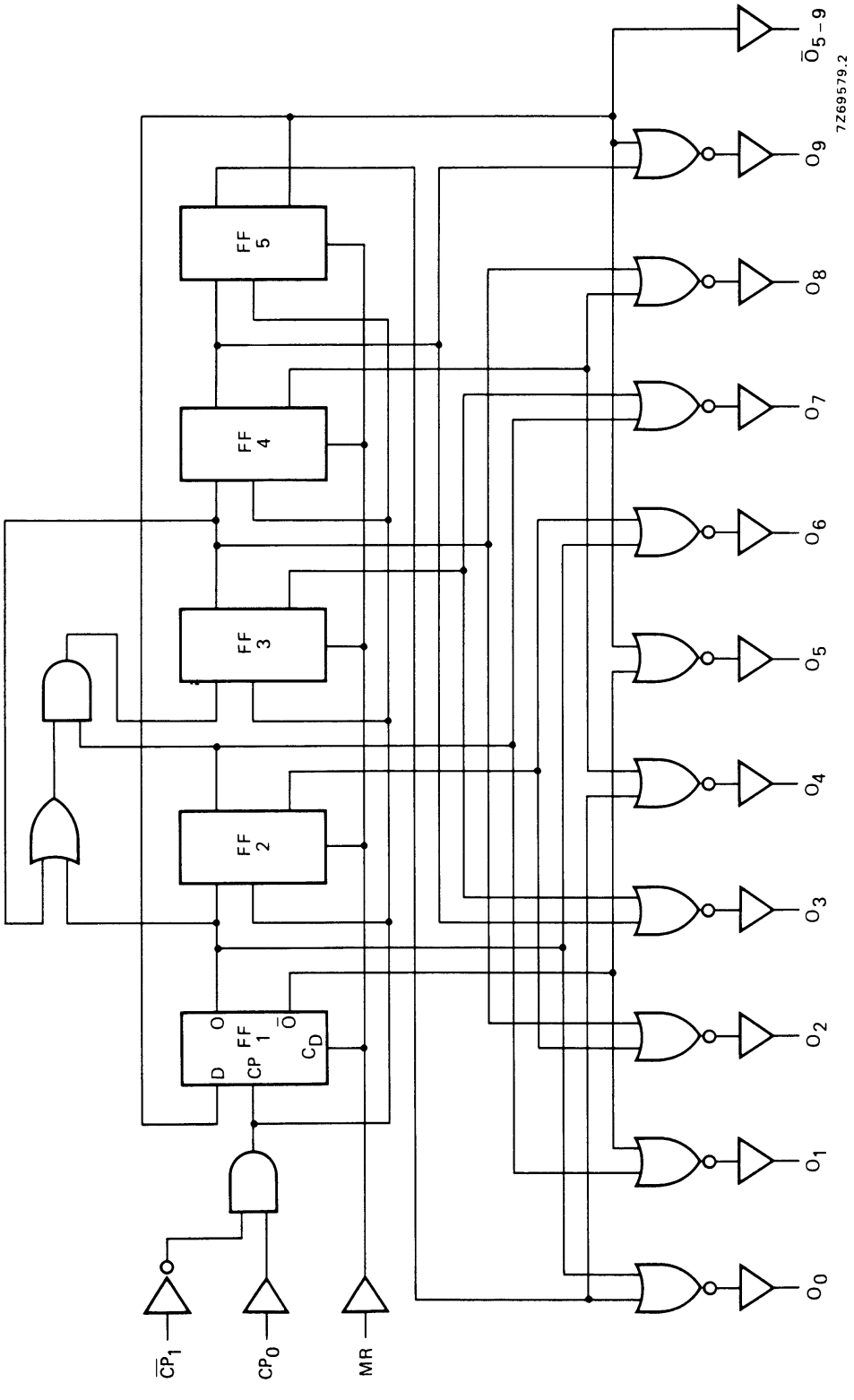



Fig.3 Logic diagram.

**FUNCTION TABLE**

| MR | $CP_0$ | $\overline{CP}_1$ | OPERATION |
|---|---|---|---|
| H | X | X | $O_0 = \overline{O}_{5\text{-}9}$ = H; $O_1$ to $O_9$ = L |
| L | H | ↓ | Counter advances |
| L | ↑ | L | Counter advances |
| L | L | X | No change |
| L | X | H | No change |
| L | H | ↑ | No change |
| L | ↓ | L | No change |

**Notes**

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4. ↑ = positive-going transition
5. ↓ = negative-going transition

**AC CHARACTERISTICS**

$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; $C_L$ = 50 pF; input transition times ≤ 20 ns

| | $V_{DD}$ V | SYMBOL | MIN. | TYP. | MAX. | | TYPICAL EXTRAPOLATION FORMULA |
|---|---|---|---|---|---|---|---|
| Propagation delays | | | | | | | |
| $CP_0$, $\overline{CP}_1 \rightarrow O_0$ to $O_9$ | 5 | | | 140 | 280 | ns | 113 ns + (0,55 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{PHL}$ | | 55 | 110 | ns | 44 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| | 5 | | | 125 | 250 | ns | 98 ns + (0,55 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{PLH}$ | | 50 | 100 | ns | 39 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| $CP_0$, $\overline{CP}_1 \rightarrow \overline{O}_{5\text{-}9}$ | 5 | | | 145 | 290 | ns | 118 ns + (0,55 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{PHL}$ | | 55 | 110 | ns | 44 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| | 5 | | | 125 | 250 | ns | 98 ns + (0,55 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{PLH}$ | | 50 | 100 | ns | 39 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| MR $\rightarrow O_1$ to $O_9$ | 5 | | | 115 | 230 | ns | 88 ns + (0,55 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{PHL}$ | | 50 | 100 | ns | 39 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 35 | 70 | ns | 27 ns + (0,16 ns/pF) $C_L$ |
| MR $\rightarrow \overline{O}_{5\text{-}9}$ | 5 | | | 110 | 220 | ns | 83 ns + (0,55 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{PLH}$ | | 45 | 90 | ns | 34 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 35 | 70 | ns | 27 ns + (0,16 ns/pF) $C_L$ |
| MR $\rightarrow O_0$ | 5 | | | 130 | 260 | ns | 103 ns + (0,55 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{PLH}$ | | 55 | 105 | ns | 44 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 75 | ns | 32 ns + (0,16 ns/pF) $C_L$ |

| | $V_{DD}$ V | SYMBOL | MIN. | TYP. | MAX. | | TYPICAL EXTRAPOLATION FORMULA |
|---|---|---|---|---|---|---|---|
| Output transition | | | | | | | |
| times | 5 | | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{THL}$ | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |
| | 5 | | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{TLH}$ | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |

**AC CHARACTERISTICS**

$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; $C_L$ = 50 pF; input transition times ≤ 20 ns

| | $V_{DD}$ V | SYMBOL | MIN. | TYP. | MAX. | | |
|---|---|---|---|---|---|---|---|
| Hold times | 5 | | 90 | 45 | | ns | |
| $CP_0 \rightarrow \overline{CP}_1$ | 10 | $t_{hold}$ | 40 | 20 | | ns | |
| | 15 | | 20 | 10 | | ns | |
| | 5 | | 80 | 40 | | ns | |
| $\overline{CP}_1 \rightarrow CP_0$ | 10 | $t_{hold}$ | 40 | 20 | | ns | |
| | 15 | | 30 | 10 | | ns | |
| Minimum clock | | | | | | | |
| pulse width: | 5 | | 80 | 40 | | ns | |
| $CP_0$ = LOW; | 10 | $t_{WCPL}$ = $t_{WCPH}$ | 40 | 20 | | ns | see also waveforms |
| $\overline{CP}_1$ = HIGH | 15 | | 30 | 15 | | ns | Figs 4 and 5 |
| Minimum MR | 5 | | 50 | 25 | | ns | |
| pulse width; HIGH | 10 | $t_{WMRH}$ | 30 | 15 | | ns | |
| | 15 | | 20 | 10 | | ns | |
| Recovery time | 5 | | 60 | 30 | | ns | |
| for MR | 10 | $t_{RMR}$ | 30 | 15 | | ns | |
| | 15 | | 20 | 10 | | ns | |
| Maximum clock | 5 | | 6 | 12 | | MHz | |
| pulse frequency | 10 | $f_{max}$ | 12 | 24 | | MHz | |
| | 15 | | 15 | 30 | | MHz | |

| | $V_{DD}$ V | TYPICAL FORMULA FOR P (μW) | |
|---|---|---|---|
| Dynamic power | 5 | $500\ f_i + \sum (f_o C_L) \times V_{DD}^2$ | where |
| dissipation per | 10 | $2200\ f_i + \sum (f_o C_L) \times V_{DD}^2$ | $f_i$ = input freq. (MHz) |
| package (P) | 15 | $6000\ f_i + \sum (f_o C_L) \times V_{DD}^2$ | $f_o$ = output freq. (MHz) |
| | | | $C_L$ = load cap. (pF) |
| | | | $\sum (f_o C_L)$ = sum of outputs |
| | | | $V_{DD}$ = supply voltage (V) |

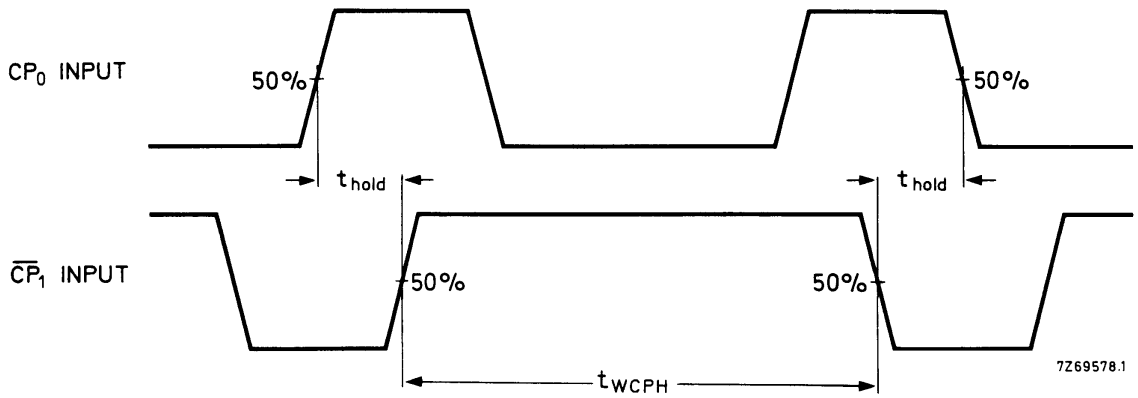
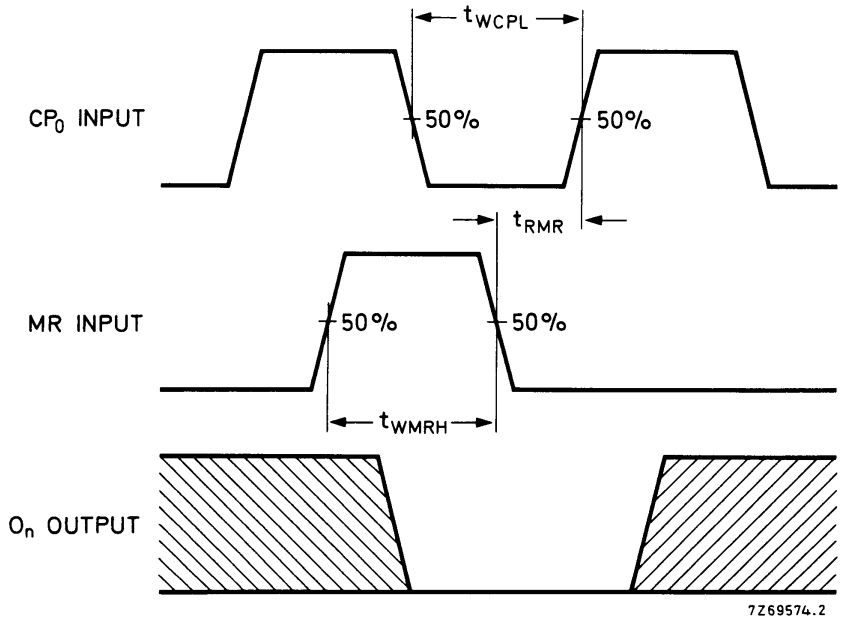



Fig.4 Waveforms showing hold times for $CP_0$ to $\overline{CP}_1$ and $\overline{CP}_1$ to $CP_0$. Hold times are shown as positive values, but may be specified as negative values.




Conditions: $\overline{CP}_1$ = LOW while $CP_0$ is triggered on a LOW to HIGH transition. $t_{WCP}$ and $t_{RMR}$ also apply when $CP_0$ = HIGH and $\overline{CP}_1$ is triggered on a HIGH to LOW transition.

Fig.5 Waveforms showing recovery time for MR; minimum $CP_0$ and MR pulse widths.

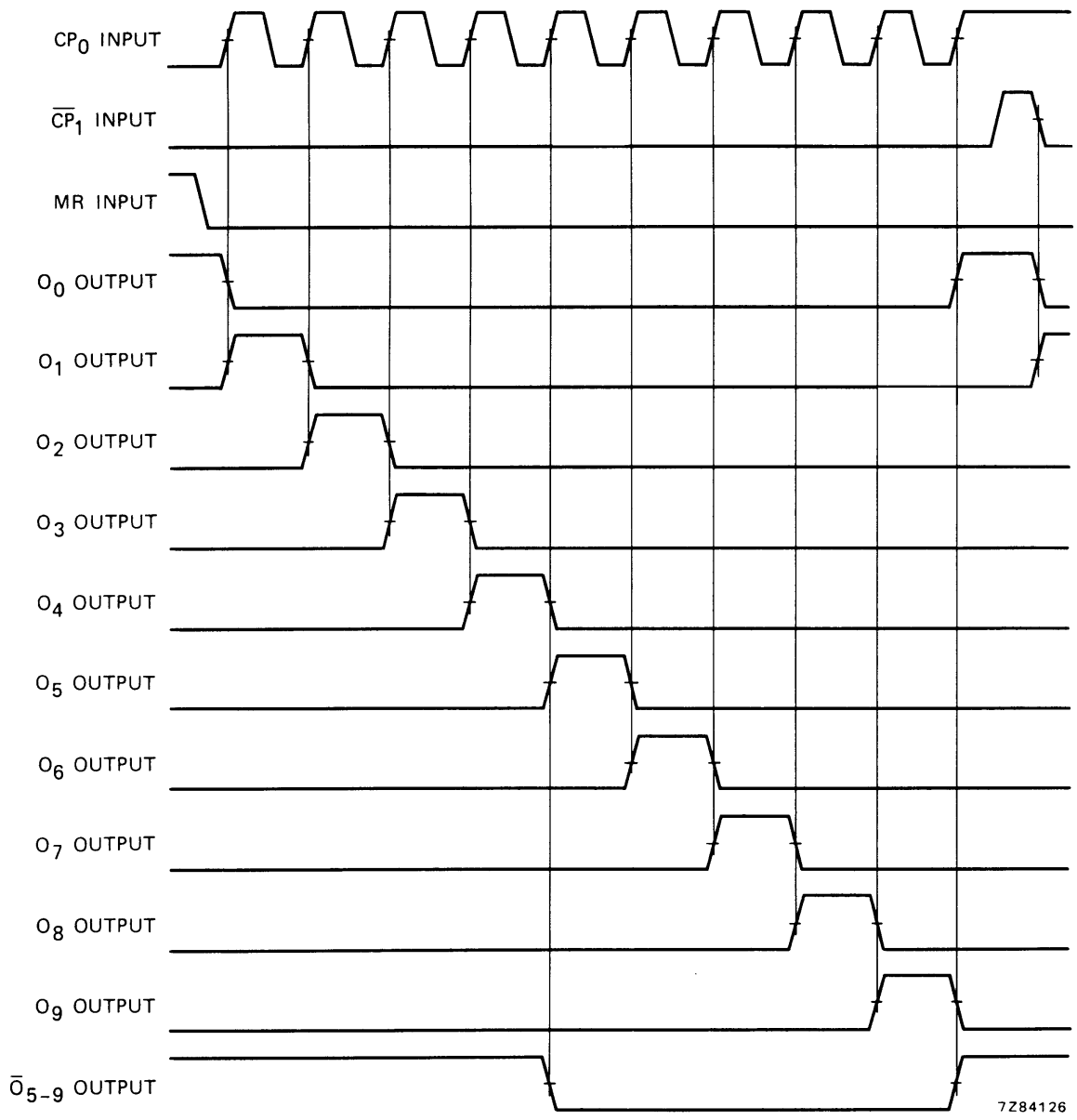



Fig.6 Timing diagram.

**APPLICATION INFORMATION**

Some examples of applications for the HEF4017B are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer.

Figure 7 shows a technique for extending the number of decoded output states for the HEF4017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

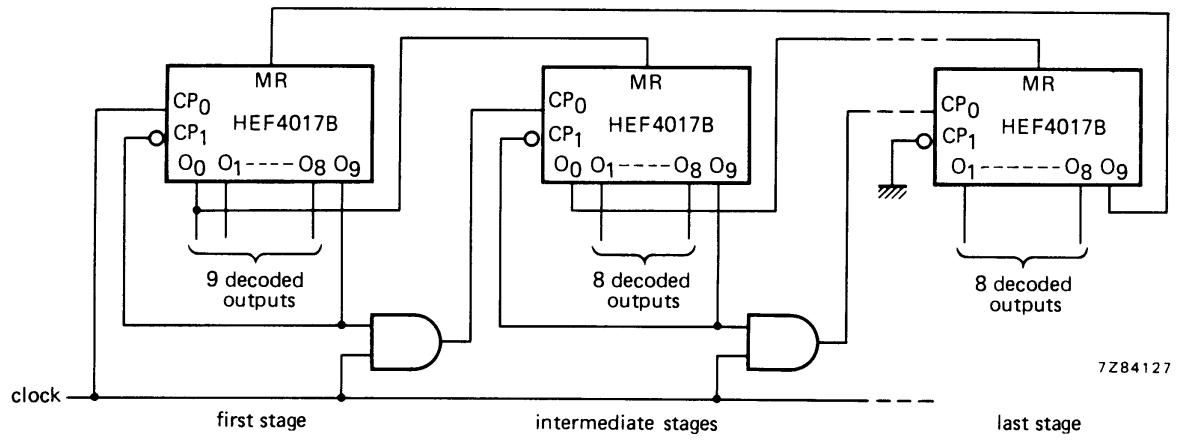



Fig.7 Counter expansion.

Note

It is essential not to enable the counter on $\overline{CP}_1$ when $CP_0$ is HIGH, or on $CP_0$ when $\overline{CP}_1$ is LOW, as the this would cause an extra count.